OIPE JC176
APR 17 2003
PATENT & TRADEMARK OFFICE

#4/ Sub Declaration 4/23/03 C.P.

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Bijan Davari, et al. **Examiner:** Long Pham

Serial No.: 09/975,435 **Art Unit:** 2814

Filed: October 11, 2001 **Docket:** YOR919990101US2 (16322)

For: PATTERNED SOI REGIONS ON SEMICONDUCTOR CHIPS

Commissioner for Patents
Washington, DC 20231

RECEIVED
APR 21 2003
TECHNOLOGY CENTER 2800

DECLARATION UNDER 37 C.F.R. §1.131

Sir:

We, Bijan Davari, Devendra K. Sadana, Ghavam G. Shahidi and Sandip Tiwari, hereby declare that:

1. We are the applicants named in U.S. Patent Application Serial No. 09/975,435, filed October 11, 2001.

2. We made the invention which is disclosed and claimed in the present application, in the United States, prior to February 25, 1999, which is the effective U.S. filing date of U.S. Patent No. 6,063,652 to Kim ("Kim").

3. As evidence of completion of said invention prior to the effective filing date of Kim annexed hereto are Exhibits A and B. Exhibits A and B consist of true photocopies of a write-up prepared by us (with hand made sketches and TEM's) as well as an IBM invention disclosure (with hand made sketches) which evidence that the claimed invention was developed in the laboratories at IBM Corporation in Yorktown Heights, NY prior to the February 25, 1999 effective filing date of Kim. The activity contributing to the development of the claimed invention was conducted by us or by other

scientists and/or technicians working under our direct supervision and control prior to the effective filing date of Kim. Dates and names have been redacted in the preparation of the photocopies contained in the attached exhibits.

4. The instant application is directed to semiconductor structures including a semiconductor substrate containing silicon having an upper surface, said substrate having at least one silicon-on-insulator (SOI) region and at least one bulk semiconductor region adjacent to the SOI region. The instant application is also directed to methods of forming the semiconductor structures of the present application. We have been advised by counsel that method Claims 35-56 are the subject matter of the instant application currently being prosecuted in the above-identified application. In broad terms, the method of the present invention comprises the steps of forming a first mask having an opening therein on a Si-containing substrate; implanting oxygen ions through the opening in the first mask into the substrate; and annealing the substrate to form a plurality of first buried oxide regions below a Si-containing layer whereby spaced apart SOI regions are formed.

In some embodiments of the present invention, the Si-containing substrate includes trenches formed therein. It that embodiment of the claimed invention, the method includes the steps of selecting a substrate containing Si having a plurality of trenches therein; forming a first mask on the substrate having an opening to expose a trench portion, and implanting oxygen through the openings into the substrate and trench portion. The implanting step employed in this embodiment includes a step of plasma immersion ion implantation of oxygen whereby the oxygen ions pass through the

sidewalls of the trench portion to form a buried oxide layer with respect to the sidewalls of the trench.

5. Exhibit A is a written disclosure that was prepared by us and submitted to counsel prior to the effective filing date of Kim. The written disclosure provides a detailed description of the present invention as well as providing further drawings that illustrate the structures and methods of the present application. In the written disclosure, it is mentioned that patterned SOI regions of the invention are formed by implanting oxygen through a dielectric mask and then annealing. Five kinds of structures containing patterned SOI regions are mentioned and shown in the hand drawn sketches.The written disclosure also includes TEMs which demonstrate that we have actually made structures using the claimed method prior to the effective filing date of Kim, i.e., prior to February 25, 1999.

6. Exhibit B is a photocopy of the invention disclosure entitled "Patterned SOI by Oxygen Implantation" along with three sheets of hand drawn sketches that were submitted by us prior to the effective filing date of Kim. The invention disclosure discusses, under the key idea of invention section, an SOI wafer and integrated circuit chip having SOI islands surrounded by bulk silicon that is formed using a mask and ion implantation. The key idea section also discusses an SOI wafer and an integrated circuit chip with a trench having horizontal and vertical buried oxide regions with respect to the wafer surface and the trench sidewalls. The hand drawn sketches show how the various structures mentioned in the key idea invention section of the original disclosure are made.

The first drawing on the first sheet shows the formation of a buried oxide region into a Si-containing substrate using a first mask and ion implantation which is

represented by the arrows. The second drawing on the first sheet shows the formation of a structure having a top Si-containing layer of variable thickness using a mask which is thin enough to allow oxygen ions to be implanted into the substrate. Note that the buried oxide region created using this method is closer to the upper surface of the substrate in the region including the first mask as compared to the buried oxide region formed in regions not containing the mask. The third hand drawn sketch shows a structure that is formed having a buried oxide region in contact with the upper surface of the substrate and other buried oxide region which is not in contact with the upper surface of the substrate. A mask and ion implantation are used in making this structure as well.

The second sheet of drawings, which includes a single figure, shows a resultant structure that can be formed using the SOI substrates provided by the claimed method.

The third sheet of drawings shows a structure including a Si-containing substrate having a trench region formed therein having horizontal and vertical buried oxides regions with respect to the upper surface of the substrate and the trench sidewalls, respectively. Note that this sketch shows ions being implanted through the upper surface of the substrate as well as the sidewalls of the trench.

7. We further declare that all statements made herein of our knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date:_____ _____

Bijan Davari

Date:_____ _____

Devendra K. Sadana

Date:_____ _____

Ghavam G. Shahidi

Date:_____ _____

Sandip Tiwari

Patent Value Tool

IBM Confidential

Title: Patterned SOI by Oxygen Implantation

Inventor:

Inventor:

Inventor:

Inventor:

Disclosure number:

Total Patent Value Tool score: 50

Key idea of invention:

An SOI wafer and integrated circuit chip with variable thickness Si according to a mask pattern. An SOI wafer and integrated circuit chip having SOI islands surrounded by bulk Si according to a mask pattern. An SOI wafer and integrated circuit chip with a silicon island bounded on all sides by oxide formed by ion implantation. An SOI wafer and integrated circuit chip with a trench having horizontal and vertical buried oxide with respect to the wafer surface and trench sidewall surfaces. An SOI wafer and integrated circuit with a silicon island or SOI island containing an FET and a decoupling capacitor in a trench in bulk silicon close by and further a substrate contact to the bulk silicon surface. A body tie contact to control floating body effects in SOI islands via the bulk silicon close by.

1. What is the anticipated annual market size (in dollars) that will be captured by your invention? >$5B

Market explanation:
SOI is an alternative to bulk Si for IC manufacturing. Bulk Si is about $150B. A 30% penetration would by reasonable.

2. How new is the technical field? Emerging

Newness explanation:

3. How central is the invention to the product(s) which might be expected to contain the invention? Essential

Centrality explanation:

4. What is the scope of the claim? Moderate

Scope explanation:

5. What are the portfolio needs in the area of your invention? PPM Needs

Portfolio needs explanation:
Matches PPM Need for 1. (CMOS Technology) Low power/high speed logic, low noise/low power high

6. How easily can the use of the invention by a competitor be detected? With Work

Detectability explanation:

7. How easily can use of the invention be avoided by a competitor? With Much Work

Avoidance explanation:

8. What percentage of the companies producing products in the field of this invention might use this invention? Broadly Cloned

Likelihood of cloning:

9. What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies? High value

Status of alliance:

10. What is the value of this patent to current or anticipated Technology Transfer Activity (between IBM and other companies)? Some value

Status of technology transfer to non-IBM partner:

11. Does it result in prestige to IBM? Industry-Wide

Prestige to IBM:

DISPOSITION: File

Standard Questions

1. Please indicate if any or all of the following apply to this invention:

Was it conceived or first actually reduced to practice under the Consortium for Superconducting Electronics? No

Was it, in any way, started or developed under a government contract or project? No

Do you consider that the material contained in this disclosure should be classified in the interest of National Security? No

Do you have a present intention to publish this subject matter? No

1. What types of companies do you expect to compete with inventions of this type? Check all that apply.
Manufacturers of mainframe computers
Manufacturers of midsize computers
Manufacturers of workstations
Manufacturers of PCs
Non-Computer manufacturers
Other (Specify)
Semiconductor manufacturers and IC foundries of low power CMOS chips

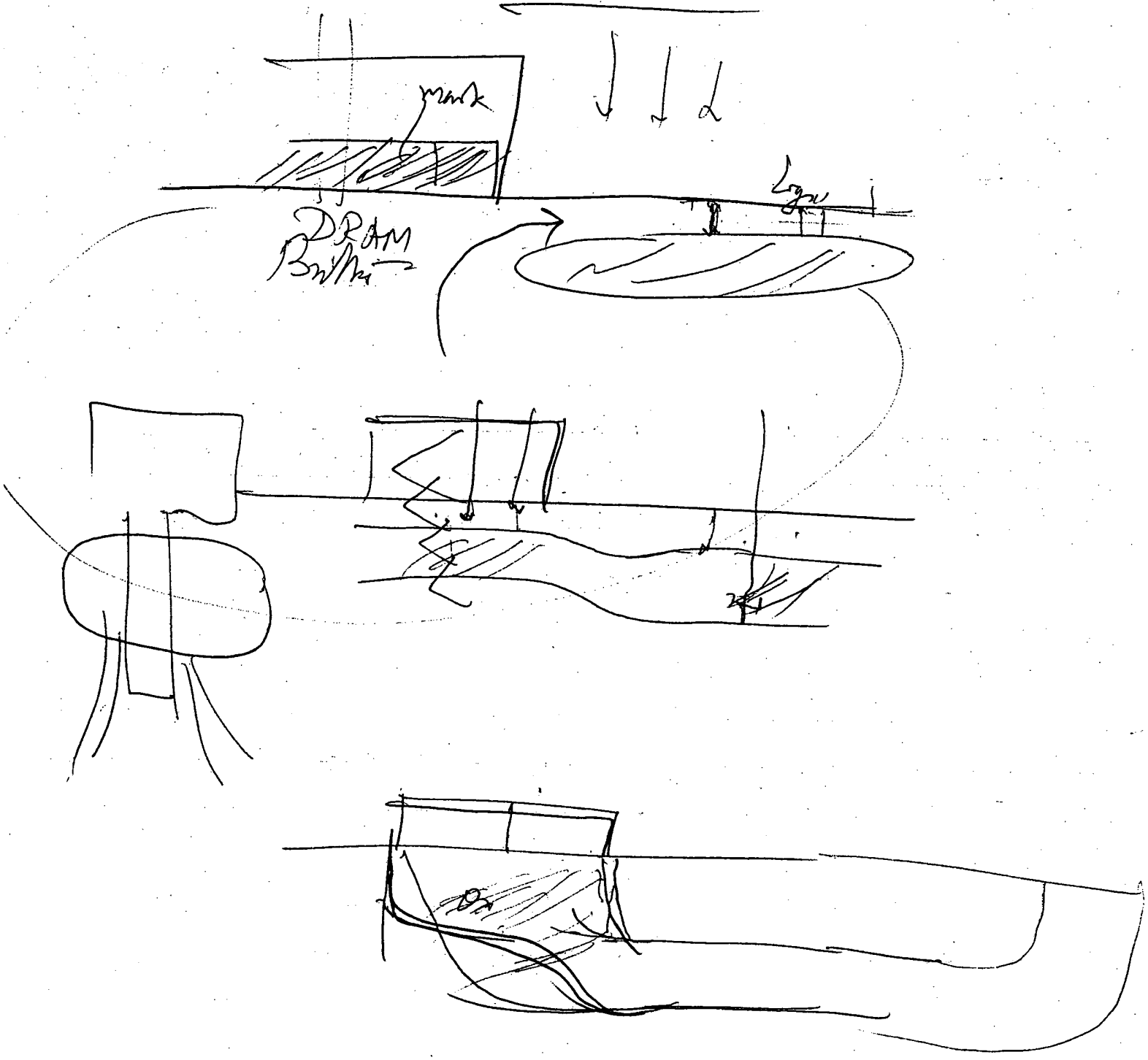
2. Please list any specific companies that you think may be interested in this patent.
Intel, NEC, AMD, Fujitsu, DEC, Samsung, HP, Motorola, etc.

Inventors' signatures:

Signature of Business Developer/Tec/Strategist:

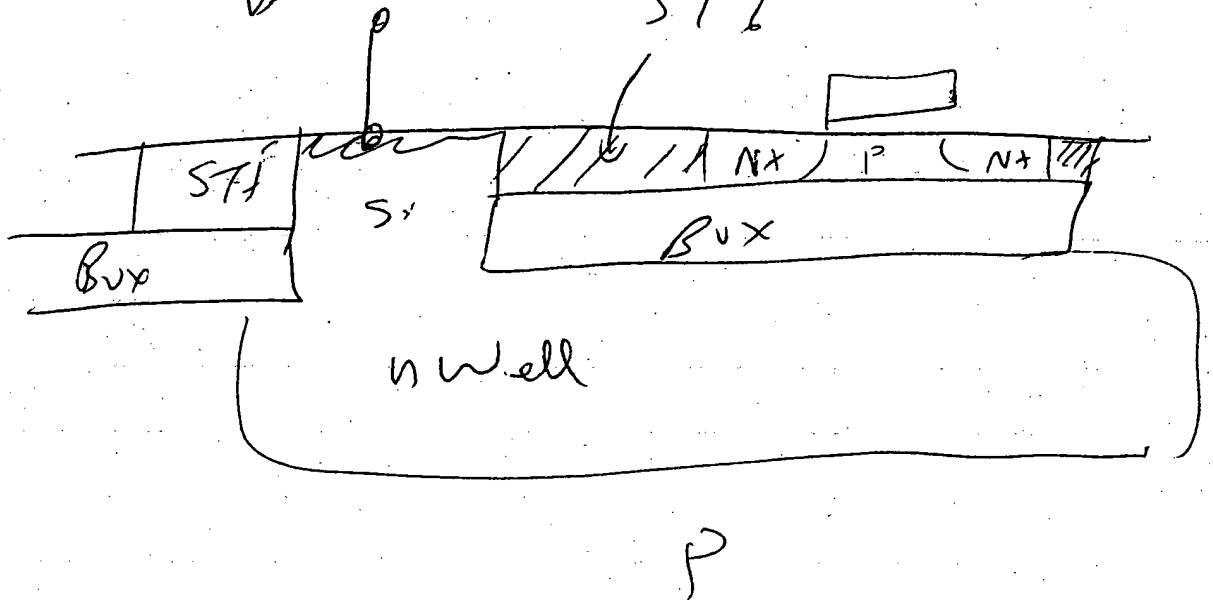
_____ Date _____

Pattern of DI

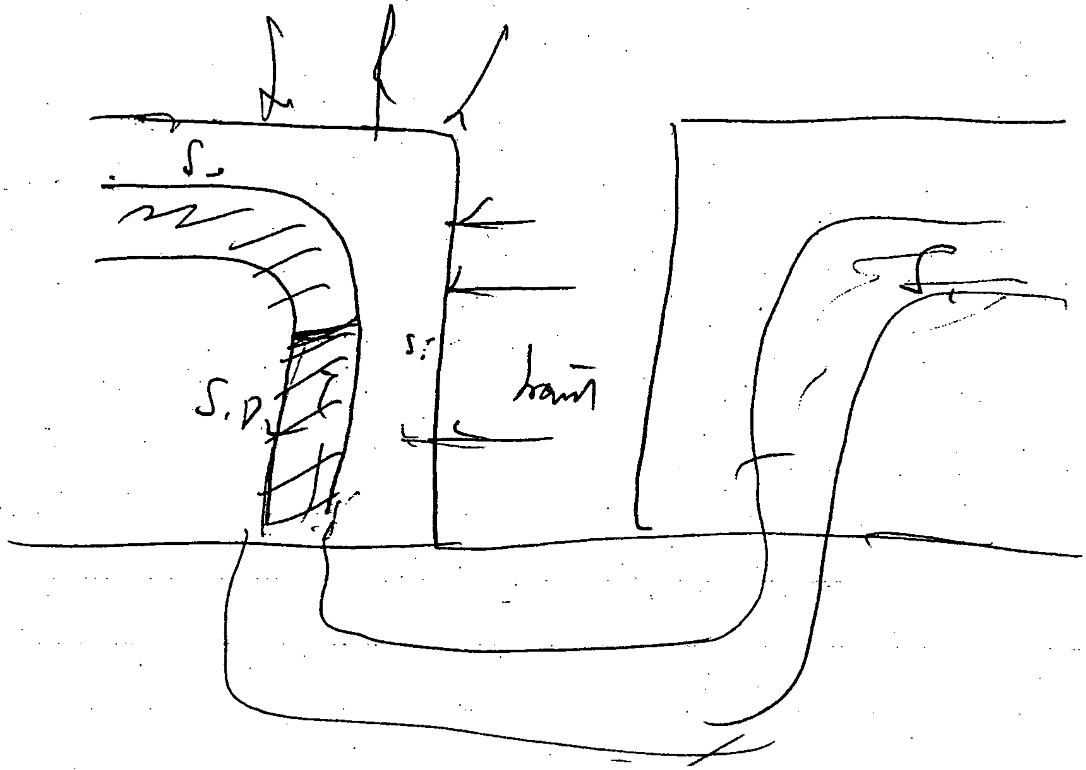


Patterned STI

Contact to substrate NW to be used for decoupling C



Patterned SPZ



PATENT APPLICATION DISPATCH SHEET

TO: Docketing Department

FROM: SUSAN FORMICOLA

The following communication (s) was sent to the U.S. Patent and Trademark Office on 4/14/03.

____ New Patent Application with transmittal in duplicate
____ Divisional ____ Continuation ____ CPA ____ CIP

____ New Provisional Patent Application with transmittal in duplicate

✓ Amendment with transmittal in duplicate

____ Preliminary Amendment with transmittal in duplicate

____ Information Disclosure Statement with PTO-1449 and copies of cited references

✓ Petition for Extension of Time ___ 1 month ✓ 2 months ___ 3 months ____
___ 4 months ___ 5 months

____ Notice of Appeal in duplicate/or Brief on Appeal in triplicate (circle one)

____ Executed Assignment with Recordal Cover Sheet in duplicate

____ Response to Notice to File Missing Parts with executed Declaration

____ Sequence Listing, Verification, Copy of Notice to Comply, Response to Notice to Comply, Computer Disk w/ Sequence in ASCII

____ Issue Fee Transmittal in duplicate

____ Transmittal of Formal Drawings (Figures _____, # of sheets _____)

✓ Deposit Account No. charged 50-0570 Amount Being Charged $ 410.00

____ Check in the amount of $ _____

✓ Certificate of Mailing ___ first class _____ Express

Other:
Unexecuted Declaration Under 1.131 w/ Exhibit A & B

Client No: _____ Client Name: _____

Serial No: _____ Docket No.: _____ Due Date: _____

Attorney Preparing Paper: _____ Attorney Signing Paper: _____

PATTERNED SOI BY OXYGEN IMPLANTATION

Introduction

It is well known that SOI based logic circuits show 20-30% higher performance than those comparably made on bulk-Si. One way to exploit this performance advantage is to fabricate ICs on patterned SOI substrates, such that logic circuits are fabricated on the SOI region whereas memories are fabricated on the bulk-Si region. Furthermore, both analog and digital circuits can be formed on SOI regions by controlling the thickness of the Si film. The patterning process also allows the formation of field isolation regions at desired locations.

Process

Patterned SOI regions in this invetion are created by implanting high doses of oxygen through a dielectric mask. In one variation, the oxygen implant and subsequent annealing conditions are equivalent to those used for standard medium or low-dose SIMOX. In another variation, the SOI regions are formed by the newly invented DIBOX process.

Patterned Structures

Five kinds of patterned SOI structures are made by adjusting oxygen beam energy, oxygen dose, and the mask material :

(i) an SOI region with the Si film thickness suitable for partially depleted devices and circuits (Fig 1)

(ii) an SOI region with Si the film thickness suitable for fully depleted devices and circuits (Fig 2)

(iii) an SOI region with Si thicknesses suitable for both partially and fully depleted devices, and their circuits (Fig 3)

(iv) an SOI region with Si thickness suitable for partially depleted devices and circuits, along with an implantion induced isolation region (Fig 4)

(iv) an SOI region with Si thickness suitable for fully depleted devices and circuits, along with an implantion induced isolation region (Fig 5).

In order to minimize surface topology on patterend regions, it is desirable to remove the dieletric mask after the oxygen implantation but before SIMOX or DIBOX annealing. Figures 6 and 7 show TEM cross-sections of a mask edge region after SIMOX and DIBOX annealing, respectively. Surface topology is within 200 Å.

In some cases it may be desirable to perform SIMOX or DIBOX annealing with the patterned make in place, such as those which require trenches.

Claims

Five kinds of patterned SOI structures are claimed by oxygen implantation of a patterned bulk-Si substrate :

(i) a patterned SOI region with the Si film thickness suitable for partially depleted devices and circuits

(ii) a patterned SOI region with Si the film thickness suitable for fully depleted devices and circuits

(iii) a patterned SOI region with Si thicknesses suitable for both partially and fully depleted devices, and their circuits

(iv) a patterned SOI region with Si thickness suitable for partially depleted devices and circuits, along with an implantion induced isolation region

(iv) a patterned SOI region with Si thickness suitable for fully depleted devices and circuits, along with an implantion induced isolation region

Fig 1

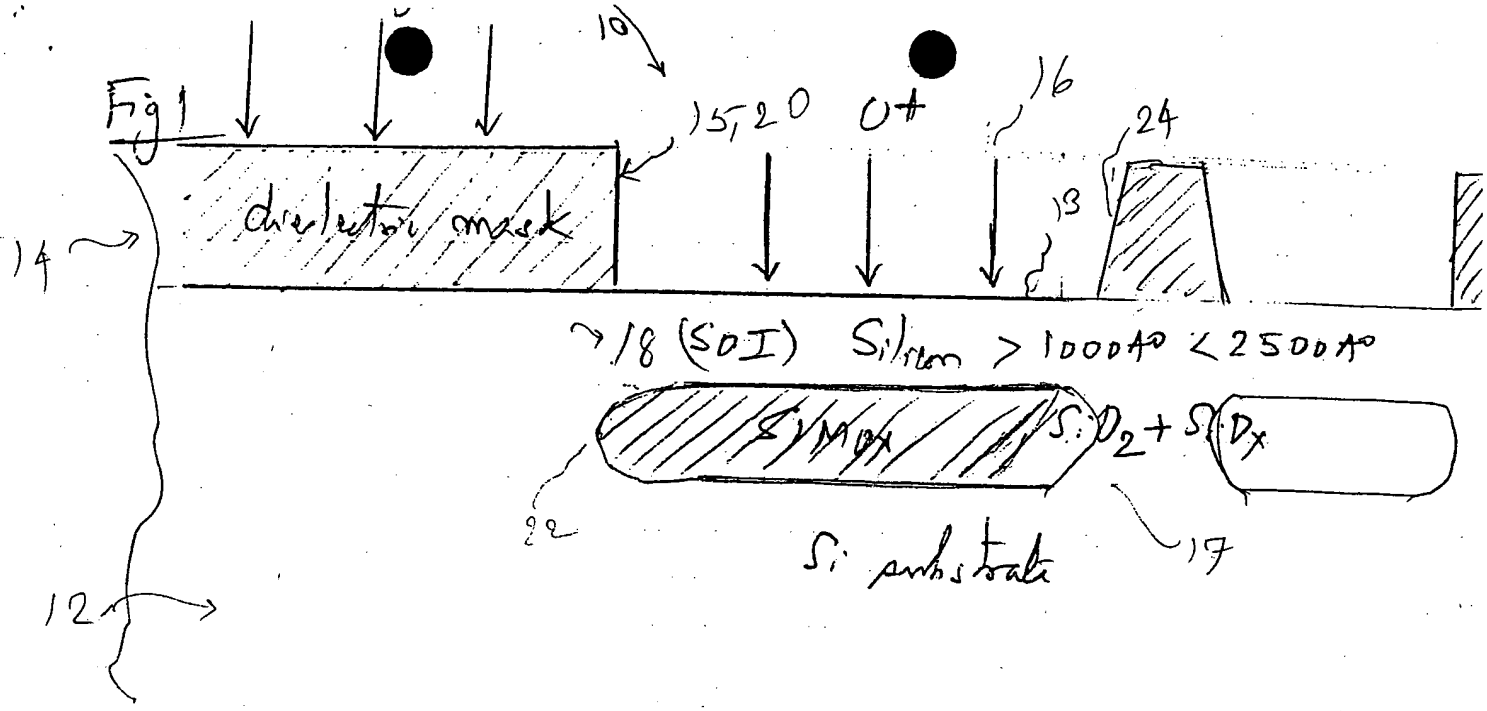

10
15, 20
16
24
dielectric mask
14
13
18 (SOI) Si film > 1000Å < 2500Å
22
Si substrate
17
12

Fig. 2

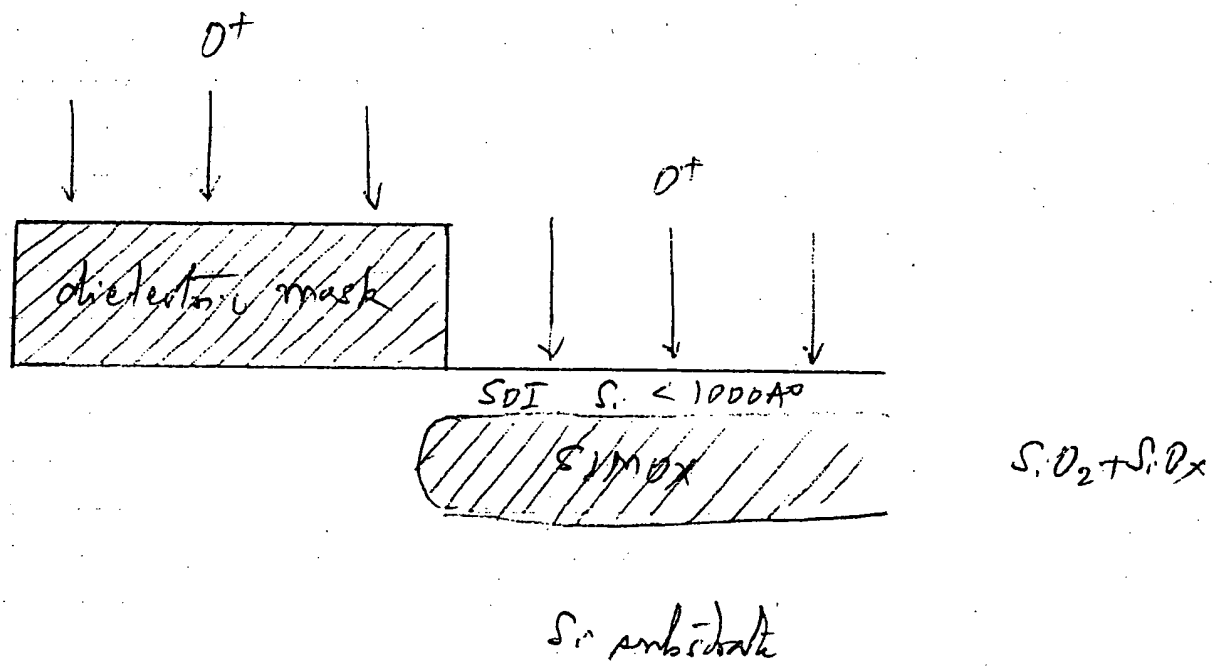


Figure 3

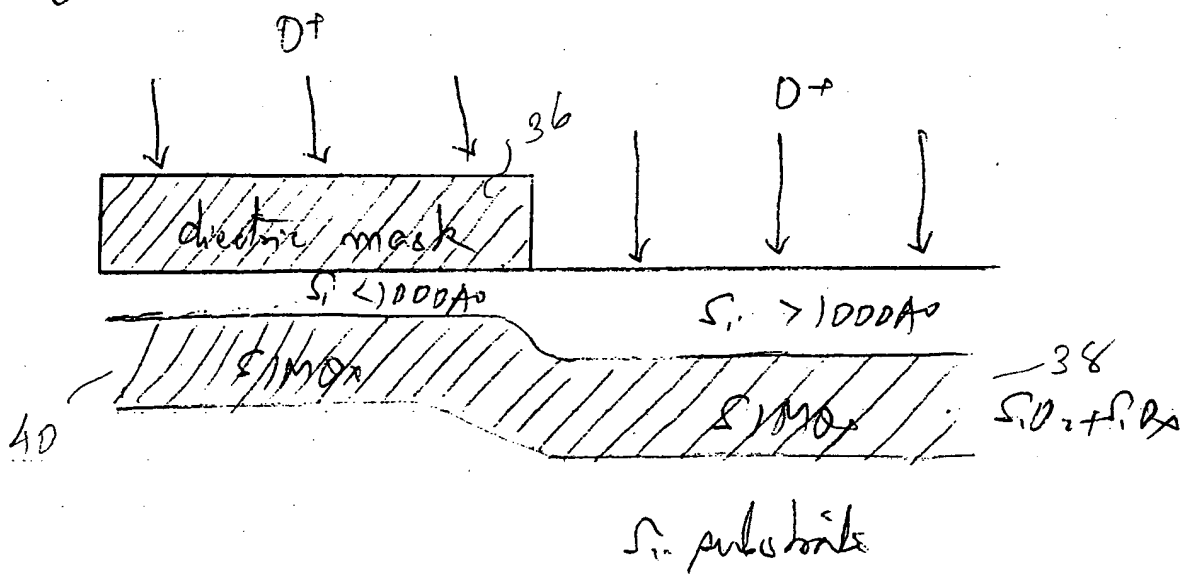

D+
D+
36
dielectric mask
Si <1000Å
Si >1000Å
SiNx
SiNx
38
SiO2+SiNx
40
Si substrate

Figure 4

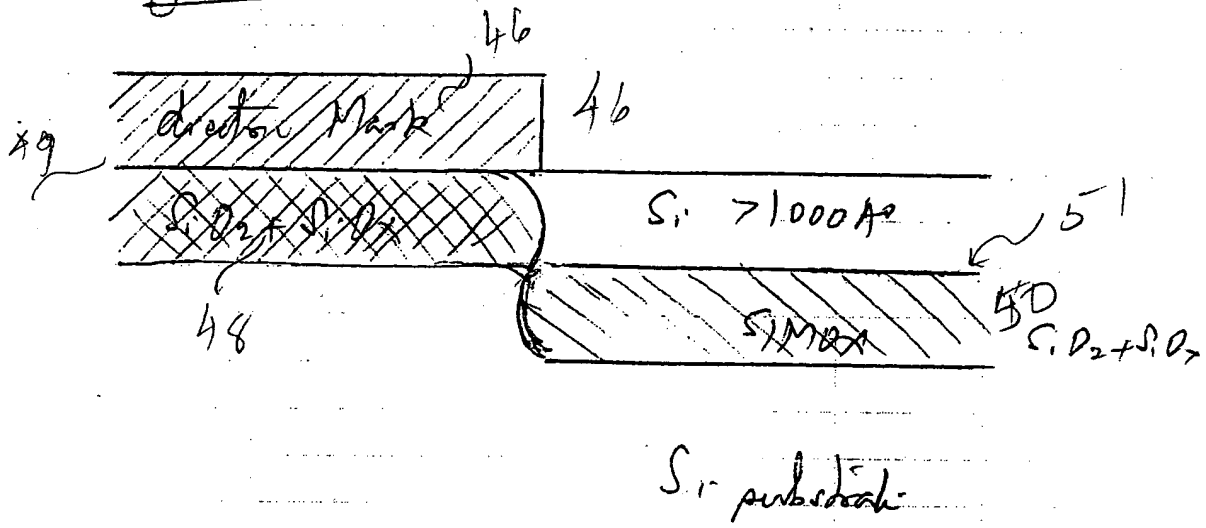
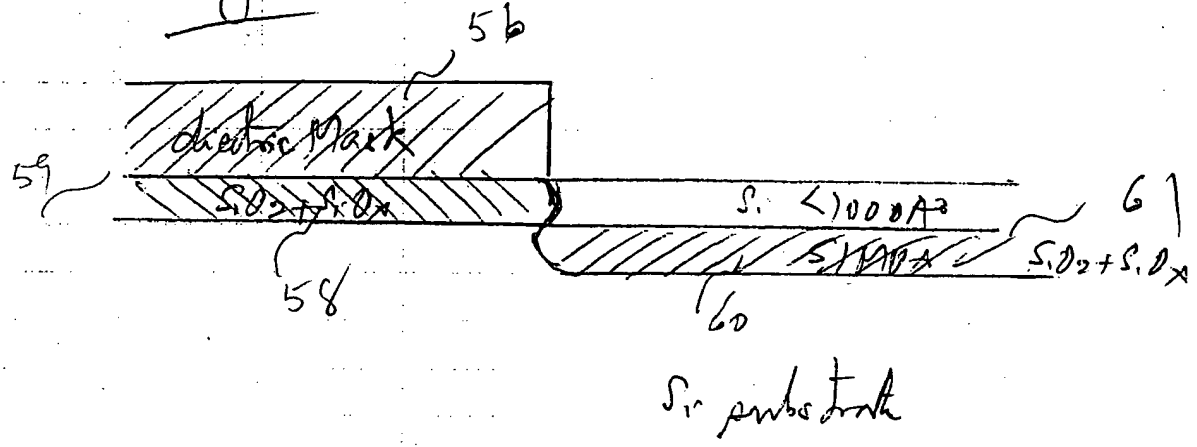


Fig. 5


5b
dielectric Mask
59
SiO2+SiOx
Si <1000Å
61
SiO2+SiOx
58
60
Si substrate

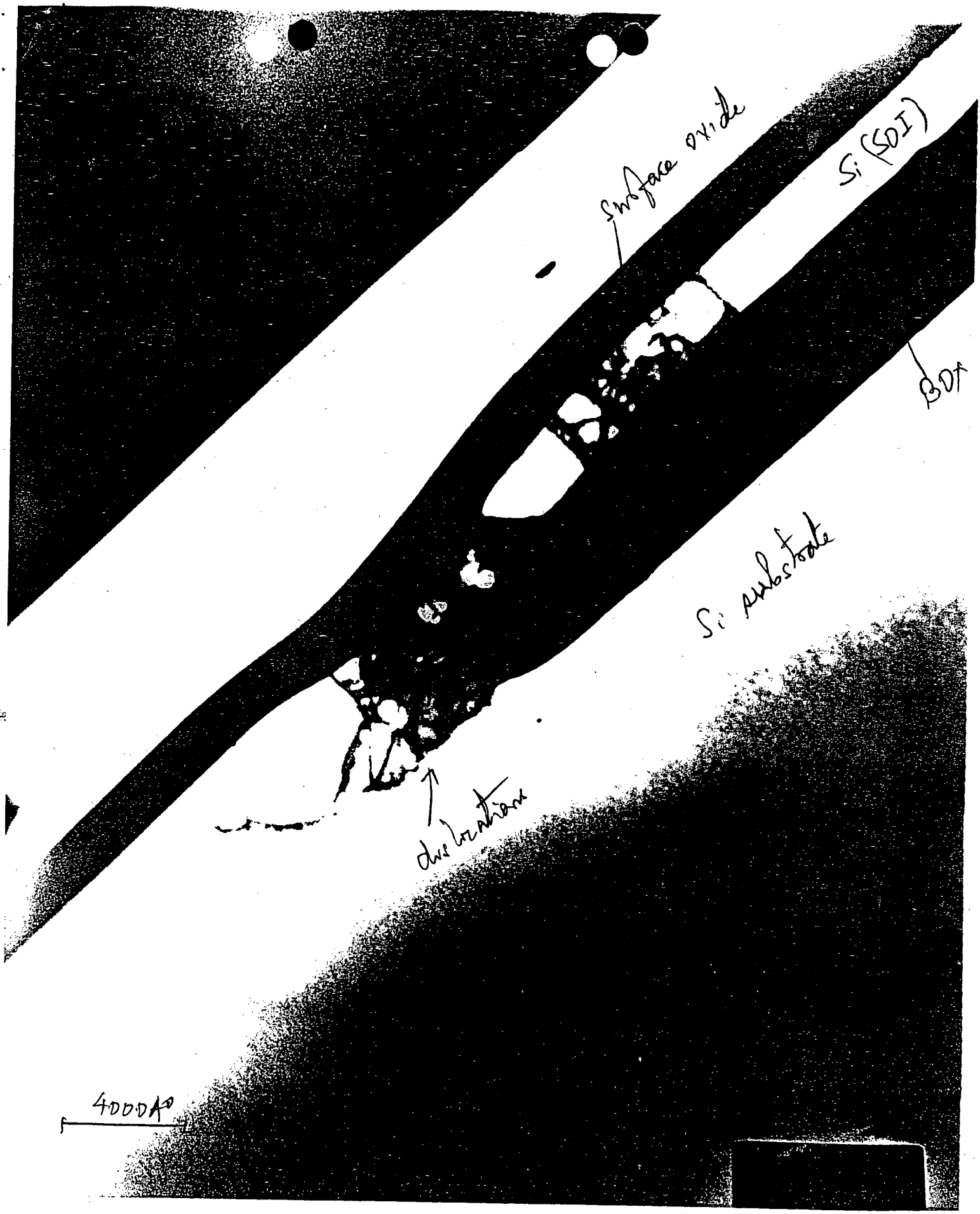


Figure 6

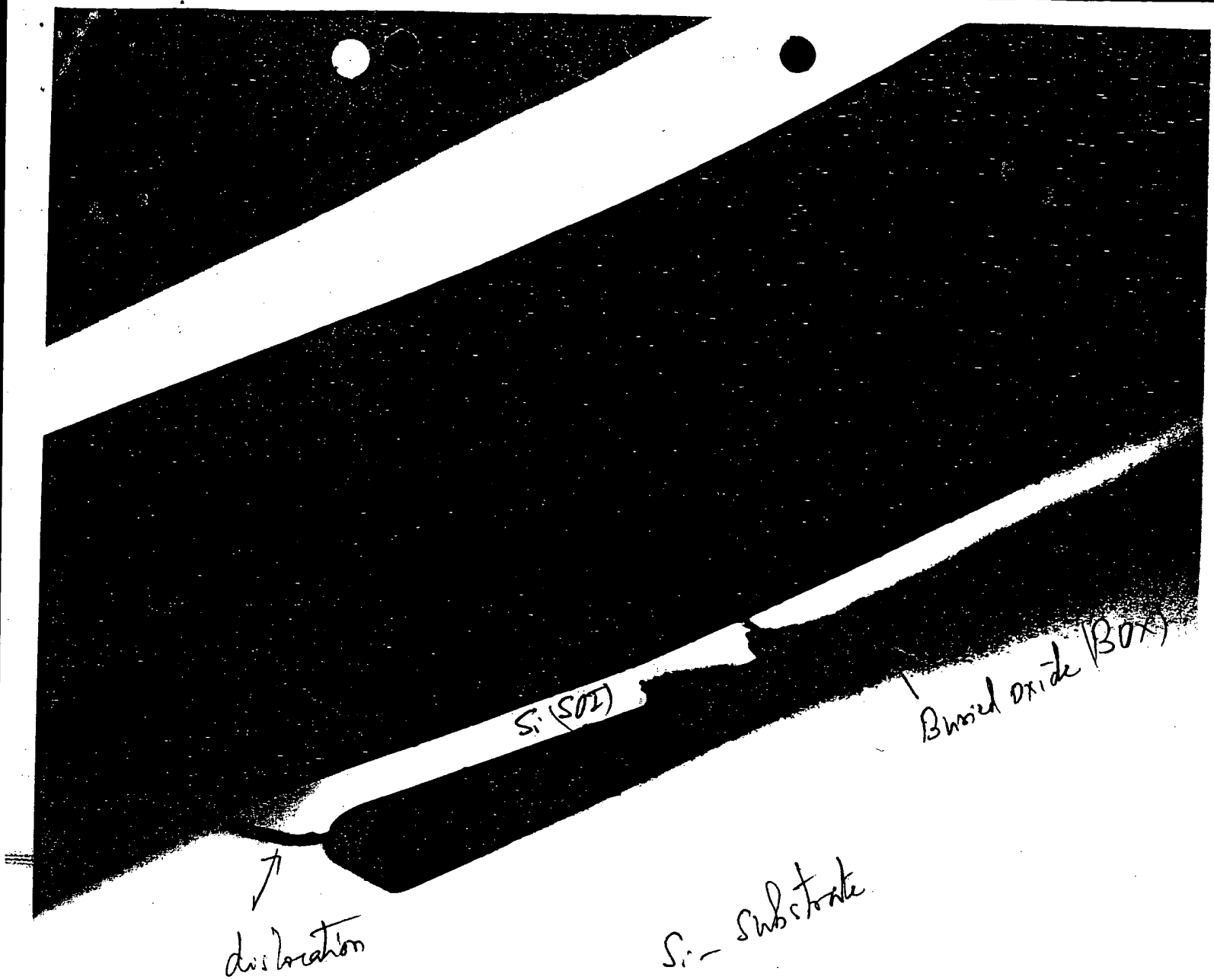


Figure 7